Amendments to the Claims:

This listing of claims will replace all prior versions and listings of claims in this application.

Listing of Claims:

Claim 1-2 (cancelled).

Claim 3 (currently amended): ~~The device of claim 2, further~~ A semiconductor device comprising:

a plurality of memory cells, at least one of the memory cells comprising:

a thyristor, and

an electrode disposed over a region of the thyristor and operable under bias to effect an electric field therein; and

a bias circuit to bias the electrode with a voltage level dependent on temperature; said device further comprising:

supporting material comprising at least one of semiconductor and conductor material;

an insulating material over the supporting material;

the thyristor formed in a layer of silicon disposed over the insulating material; and

dielectric disposed between the electrode and the layer of silicon;

the bias circuit operable to define the voltage for the electrode relative to that of the supporting material.

Claim 4 (currently amended): ~~The device of claim 1, the thyristor further~~ A semiconductor device comprising:

a layer of silicon disposed in insulated relationship over a supporting substrate;

a plurality of memory cells, at least one of the memory cells comprising:

~~the~~ a thyristor comprising N-P-N-P doped regions in the layer of silicon for respective cathode-emitter, P-base, N-base and anode-emitter regions of the thyristor~~;~~ , and

~~the~~ an electrode capacitively coupled to one of the N-base and P-base regions; and

a bias circuit to sense a temperature and vary the voltage level for a bias to ~~the bias circuit to adjust the bias of~~ at least one of the electrode and the supporting substrate dependent on the temperature.

Claim 5 (currently amended): The device of claim 4, the bias for the electrode to influence carriers in the base region ~~therebelow~~ dependent on the temperature sensed.

Claim 6 (currently amended): ~~The device of claim 1~~ A semiconductor device comprising:

a plurality of memory cells, at least one of the memory cells comprising:

a thyristor, and

an electrode disposed over a region of the thyristor; and

a bias circuit to bias the electrode with a voltage dependent on a temperature, the bias circuit to influence a gain of a bipolar device of the thyristor dependent on the temperature.

Claim 7 (previously amended): The device of claim 6, further comprising:

a support substrate comprising at least one of semiconductor and conductive material;

a dielectric over the support substrate;

a layer of silicon over the dielectric;

doped regions in the layer of silicon defining the thyristor;

the bias circuit comprising:

a temperature sensor to sense a temperature; and

a variable source to source a voltage level for the bias of at least one of the electrode and the support substrate based on the temperature sensed.

Claim 8 (currently amended): A thyristor memory device, comprising:

a thyristor formed in semiconductor material, the thyristor comprising:

an anode/cathode,

a cathode/anode, and

first and second base regions disposed in contiguous series relationship between the anode/cathode and the cathode/anode;

an electrode over one of the first and second base regions and operable under bias to affect an electric field therein; and

a temperature dependent bias circuit to bias the electrode with a voltage dependent on the temperature.

Claim 9 (original): The device of claim 8, the temperature dependent bias circuit to sense a temperature and establish the bias for the electrode with one of a positive or negative voltage-temperature coefficient of dependency.

Claim 10 (previously amended): The device of claim 9, further comprising:

a supporting substrate comprising silicon;

an oxide over the supporting substrate;

a layer of silicon over the oxide;

the thyristor formed in at least a portion of the layer of silicon; and

dielectric between the electrode and the layer of silicon;

the temperature dependent bias circuit to sense a temperature and set the bias level of at least one of the electrode and the supporting substrate based on the temperature sensed.

Claim 11 (currently amended): The device of claim 8, in which

the thyristor comprises a bipolar transistor comprising a gain (beta) that is dependent on temperature with a first gain-versus-temperature coefficient of dependency;

the temperature dependent bias circuit is operable to change the bias level of the electrode dependent on temperature to affect the gain of the bipolar transistor with a second gain-versus-temperature coefficient of dependency; and

the second gain-versus-temperature coefficient of dependency is to counter the first gain-versus-temperature coefficient of dependency.

Claims 12 - 27 (cancelled).

Claim 28 (currently amended): ~~The device of claim 27, further~~ A semiconductor memory device comprising:

a supporting substrate; ~~and~~

an insulating layer over the supporting substrate;

~~the~~ a thyristor comprisesing N-P-N-P doped regions in contiguous serial relationship in a layer of silicon over the insulating layer~~;~~, the N-P-N and the P-N-P sequences of the thyristor representative of respective bipolar transistors; and

~~the~~ means for setting ~~the~~ a bias ~~level is~~ voltage of the electrode dependent on temperature to establish an electric field through the base region between the electrode and the supporting substrate, and to influence a gain of its respective one of the N-P-N and P-N-P bipolar transistors dependent on the temperature.

~~the means for setting the bias level is operable to influence the gain of the bipolar transistor based on temperature an compensate for an intrinsic gain versus temperature dependency thereof.~~